Ferrite “detail” – Tips and Tricks.

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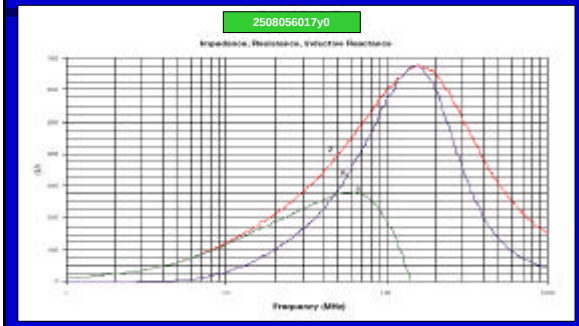
Topics of Discussion

1. The Bias effect of differential mode ferrite filtration.
2. Ferrite size / volume is important.
3. Multi-turn configurations.
4. Cancellation effects of common mode chokes.
5. Where do we use chip beads in circuits.

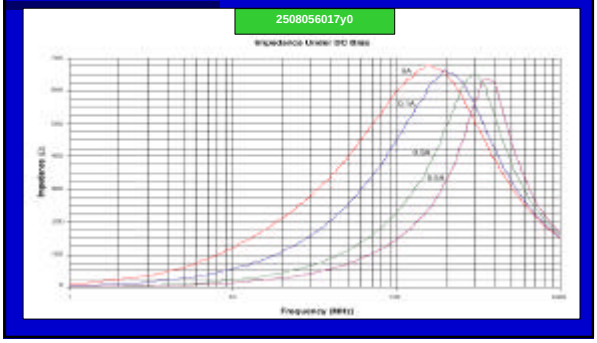
1. The Bias effect of differential mode ferrite filtration

Typical Z vs. F response of diff mode chip bead impeder. Showing Impedance, Inductive Reactance and Effective Resistance



1. The Bias effect of differential mode ferrite filtration

Same part with various levels of test bias currents, notice three things, peak Z amplitude, peak Z frequency and Q.



1. The Bias effect of differential mode ferrite filtration

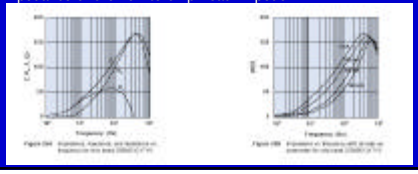
What are the implications of this ?

Impedance will not be as expected when there is a DC or AC signal present – attenuation levels will not be as expected – another design iteration may be required.

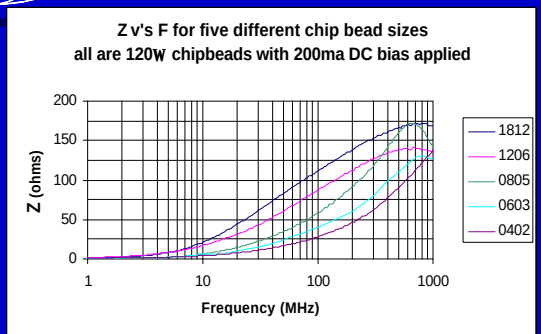
What is the solution ?

Use the Bias graphs for the initial design stage. (as per catalog)

Take into account the signal current and how that will affect the Impedance of the Ferrite Chip Bead Impeder.



2. Ferrite size / volume is important



2. Ferrite size / volume is important

What are the implications of this ?

If a design is changing passive component sizes from say 1206 to 0603 and assuming that signal levels remain at a similar amplitude then Impedance will be lower than previously seen, possibly leading to compliance issues.

Alternatively, if bench testing with a 1206 part results in a solution and the production PCB is designed to use an 0603, then Impedance on the production parts will be lower than seen in the bench testing.

What is the solution ?

If for instance the design is changing from a 1206 120ohm chip bead to an 0603 size, use a 150ohm or 200ohm or 220ohm 0603 part.

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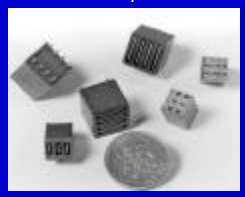
3. Multi-turn configurations

- Cable Cores and Multi-line PC Beads can be “wound”, in multi-turn configurations.
- This can result in an N^2 increase in Impedance, however there will also be a shift in peak Z.



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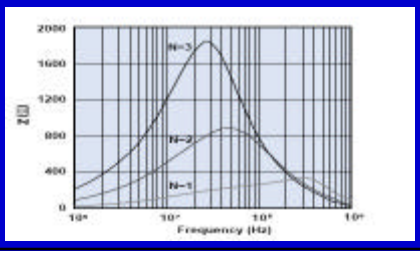
3. Multi-turn configurations

- The Graph shows the effects of adding additional turns to a 14 x 6 x 28mm core in 43 material, why does this happen ?



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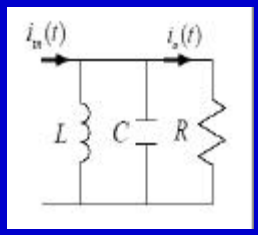
3. Multi-turn configurations

The equivalent circuit of the ferrite can be expressed as a parallel resonant circuit with a resonant frequency given by the formulae below. Adding further turns increases the Inductance and the Inter-Winding capacitance of the circuit. Thus if L & C increase fp must reduce.



$$fp = \frac{1}{2\Pi\sqrt{LC}}$$

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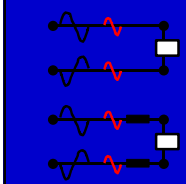
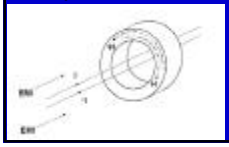
4. Cancellation effects of common mode chokes.





Consider the standard 2 wire differential circuit. The black signals represent differential mode signal (the intended signal) and the red signals represent common mode signals or CM noise.
Thus the differential mode signals are 180 degrees out of phase and the CM signals are in phase.

Now consider using differential mode filtering for this circuit. (on either or both lines of the circuit) Using differential mode filtering can in some instances lead to saturation of the ferrite core. (The DM and CM signals may be in phase)

Finally, consider a Common Mode Choke rather than one or two DM Chokes.
In a CM Choke configuration the majority of the DM Flux will be cancelled in the ferrite core due to the fact that these fluxes are 180 degrees out of phase and that they are equal in amplitude. Thus only the CM Flux will remain in the ferrite core, saturation of that core would be very unlikely.

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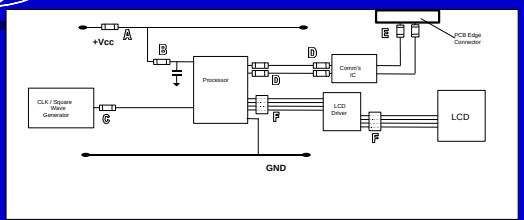
5. Where do we use chip beads in circuits?



A: To attenuate DC-DC converter switching noise and coupled digital noise present on Vcc line.
B: Attenuation of broad-band noise generated when Semiconductor device “wakes” and Icc switches from its low “sleep” current to a higher “on” current.
C: To attenuate high frequency harmonics of CLK frequency. e.g. if Clock is a 40MHz fundamental, the 5th Harmonic can be a 200MHz EMI signal.
D: To attenuate high frequency conducted noise on bi-directional data I/O lines.
E: To attenuate wide band noise present on connecting cable and to prevent conducted noise from internal circuitry transmitting onto external cable.
F: To attenuate high frequency conducted noise on bi-directional or uni-directional data lines.

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