

REGINA Test mask : Research on EMC Guidelines for INtegrated Automotive circuits

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Abstract :

This paper presents the results obtained with a specific test mask designed at Motorola for the study of the electromagnetic parasitic emissions in Integrated Circuits (IC). First, origins of parasitic emissions are presented for CMOS circuits, and ElectroMagnetic Compatibility (EMC) measurements of IC emissions are detailed: a radiated measurement method with respect to the IEC61967-2 standard and a conducted one with respect to the IEC61967-4 standard. The REGINA test chip is then described, with a focus on particular structures allowing to test and verify some design guidelines for EMC, like delay cell, emissive structure or on-chip sensor. The printed circuit board that is use to implement the test chip and the experiment test bench are also described. A set of measurements is presented and some guidelines are deduced and recommended as design rules.

Keywords :

EMC for IC, EMI, Parasitic emission, Radiated and Conducted measurements,

Modeling, CMOS circuits.

1. Introduction

The ElectroMagnetic Compatibility is nowadays one of the major causes of the redesign in microelectronics. Indeed, the electronic systems have now conquered all the industrial domain, from entertainment, communication, house applications up to transportation. In the latter domain, the ElectroMagnetic InCompatibility could have very dramatic consequences on the safety. Looking at the automotive history, the EM constraints were initially applied at the car level. Theses constraints have then been translated and applied to the electronic equipment and are now reaching microelectronic devices. To

reduce the emission of a system, the only solution is to take into account the EMC at IC level. Figure 1 illustrates the EMC environment given to an IC designer.

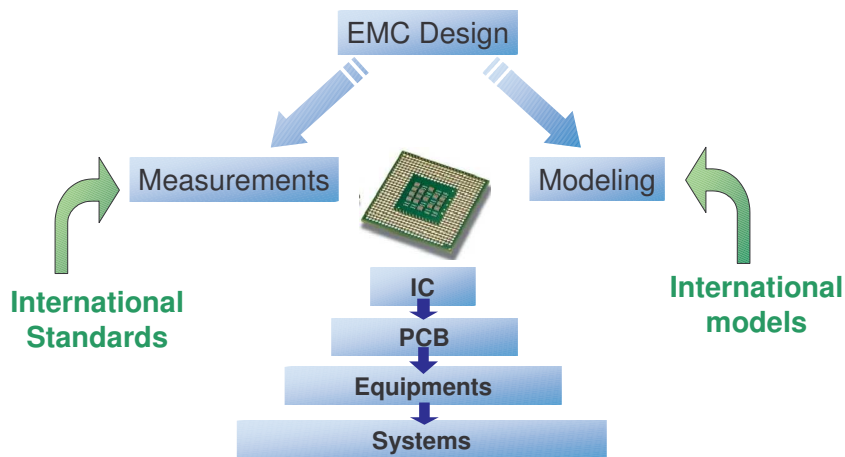


Figure 1 : The EMC context

However, the interest in the EMC for IC is rather new and is mainly due to the convergence of two industrial and technological trends:

- Integration of more complex functions, which were at the board level in the past, into the IC. These functions, analog for most of them, are often the main parts of the electronic equipment and are very sensitive to the EMC.
- Development of the technology, which allows integrating millions of logic gates working at faster rates. This integration capability has in fact increased the current consumption of the IC, and mainly its dynamic consumption [1] (see Figure 2).

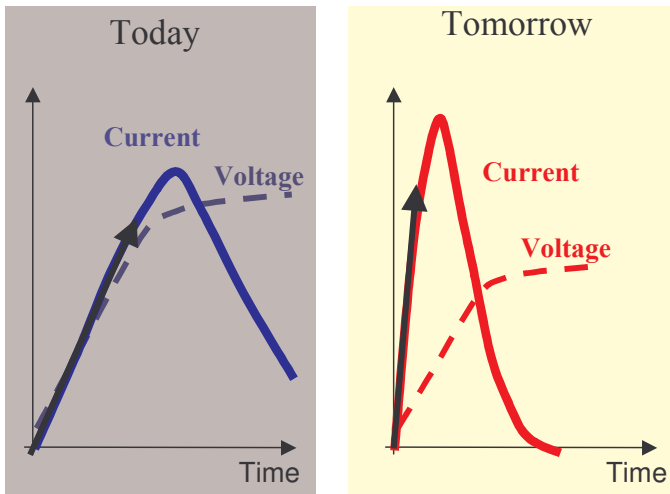


Figure 2 : Comparison of the dynamic supply current

The EMC is therefore a new area for the microelectronic industry and researches have started on this field [2] [3] [4] [5] [6] [7] [8]. The understanding of the electromagnetic emission in a chip is now achieved and is the subject of the next section.

2. Origin of the Electromagnetic Emission in a chip

The origin of parasitic emission in CMOS integrated circuit is mainly the current flowing in each elementary gate, when its output is activated, either rising from logic level 0 to 1 (Figure 3-a) or falling from 1 to 0 (Figure 3-b).

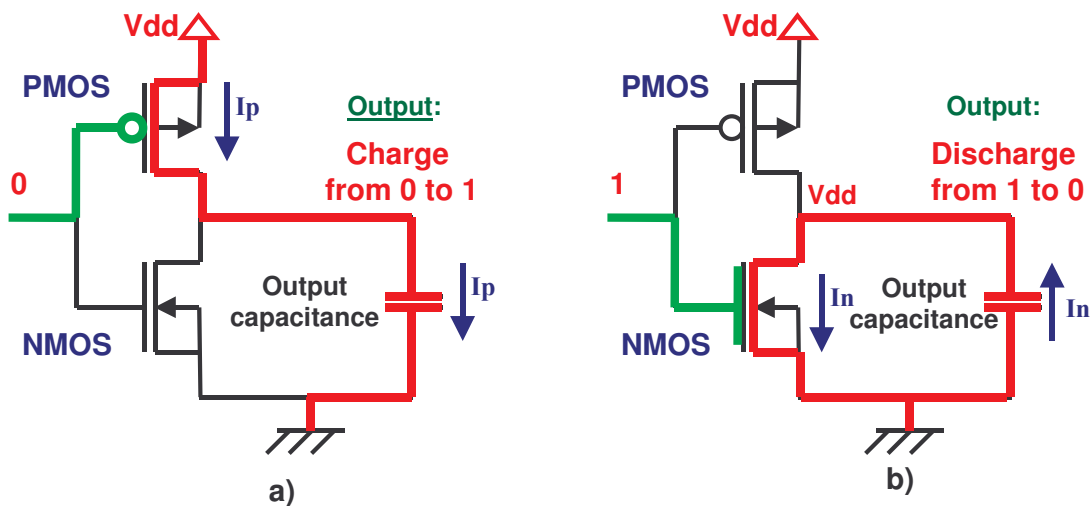


Figure 3 : Basic mechanism of parasitic emission originates from elementary current flowing during gate switching

These rapid switches give rise to very short and sharp current peaks (less than 1 ns in today's sub-micron technology) that are the sources of radiated or conducted emission. The Figure 4 shows the time domain aspect of such current measured on the power supplies of an elementary gate. On this curve, we can notice that the current begins by decreasing and becomes negative. This phenomenon is called short-through current and appears when the output of the inverter is switching from the high level to the low one. It is explained by the MOS parasitic capacitances, which exist between the output and the input of the inverter.

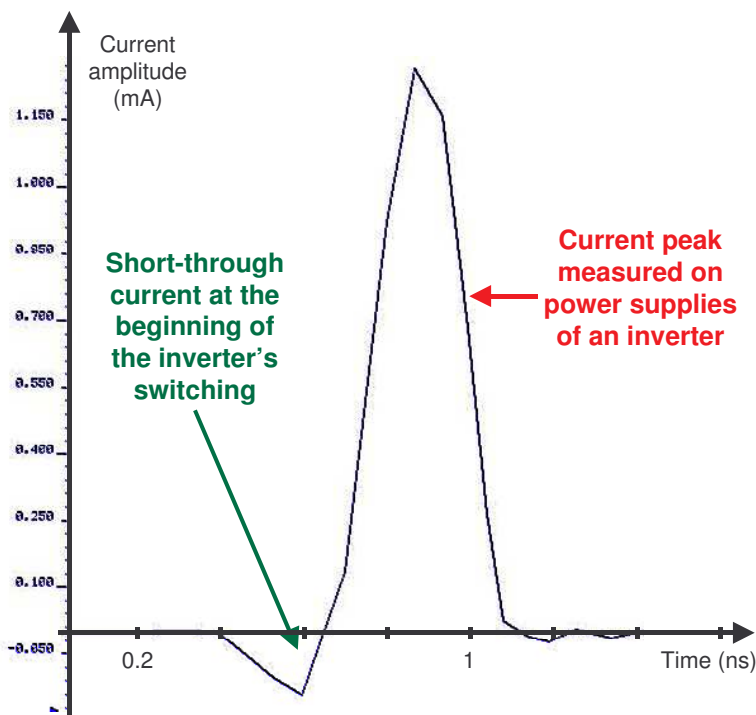


Figure 4 : Current peak generated on power supply by an inverter

The frequency aspects of such peaks can be obtained by using a Fast Fourier transform [9]. If we represent the peaks like pulse train (Figure 5—top schematics), the corresponding magnitude spectrum is shown on Figure 5 (bottom schematics) with rise time τ_r equals fall time τ_f .

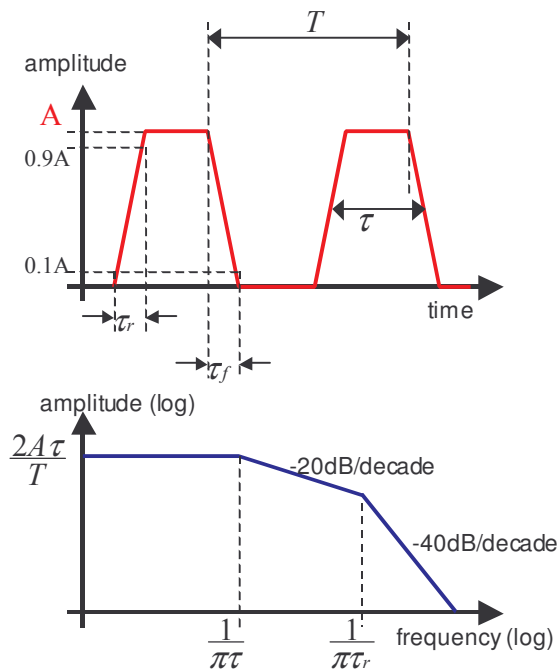


Figure 5 : Pulse trains and their frequency aspect

Therefore the sharper the peak (τ and τ_r are small compared to T) the higher the -20dB/dec and -40dB/dec cut-off frequencies where the emission spectrum envelope level start to decrease significantly. Likewise, the taller the peak in amplitude, the higher the initial emission level.

3. Measurement standards for Electromagnetic emission of component

Over the last past years, many researches have been done on the EM measurements of the Integrated Circuits. In the International Electrotechnical Commission (IEC), the technical committee TC47A is dedicated to the semiconductor products. The Working Group WG9 within this committee is specialized in the EMC measurements for the ICs. Today, many standards are available (finalized or still in a draft version). In the present work, two major methods have been used.

The first one is a radiated method (IEC61967-2) [10] [11]. The TEM Cell (for Transverse Electromagnetic Mode) is a Faraday Cage in which a 50 Ohm adapted transmission line is widen (see the Figure 6) and named septum.

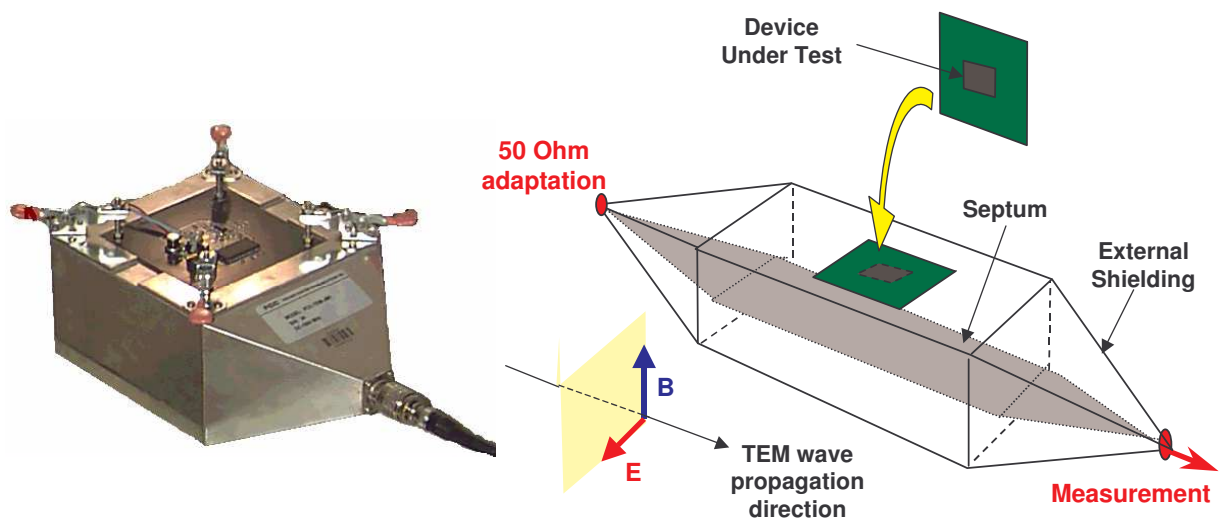


Figure 6 : The TEM Cell

A specific board (103 x 103 mm, with 4 metal layers) allows inserting the device under test in the Faraday Cage. The emission produced by the device is lightening the septum, one of whose port is connected to a spectrum analyzer. The advantage of this method is the isolation of the device under test from the other associated components and from the tracks of the PCB, allowing measuring only the component emissions. The orientation of the device under test inside the TEM Cell has also an important effect on the emissive spectrum : generally, two measurements with two different orientations have to be done [12].

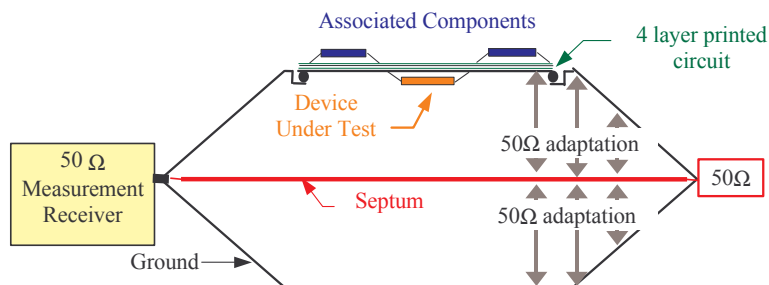


Figure 7 : Section of the TEM Cell with the device under test

One of the disadvantages of the TEM Cell is that there are preferred coupling orientations between the component and the septum that may enhance or minimize some specific emissions. Some studies are under way to build a 3D TEM Cell (with 6 septums, 2 septums on each x,y,z axes) [13] [14] to avoid such misrepresentations.

The second method is a conducted measurement (IEC61967-4) [15] [16] [17]. The principle of this method is based on the current loop : switching and voltage variations in the IC create RF currents that are propagated outside the IC through I/O and power supplies and generate the electromagnetic emission of the component. These currents return back inside the component through the ground link. Measuring the current variations on the IC ground therefore gives an image of the EM emission of the component. The Figure 8 highlights this method.

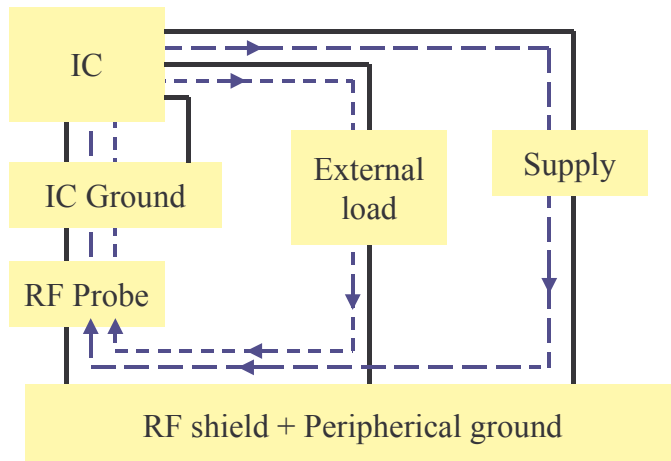


Figure 8 : Conducted method

Moreover a correlation has been shown between this conducted measurement and the radiated emission of the IC. [18]. In the case presented here, measurements have been performed only on the power supply. The standard proposes that a resistance of 1 Ohm could be used as the RF probe. More details on this probe could be found in the standard.

These two measurements methods have been applied for the evaluation of our test mask in a frequency range from 1MHz up to 1 GHz. Therefore we will give more details on the Printed Circuit Board in the corresponding paragraph, which has been designed in accordance with these standards.

4. Description of the specific test chip REGINA

The REGINA test chip [19] [20] (REGINA stands for Research on EMC Guidelines for INtegrated circuits in Automotive) has been designed to validate some rules for low emission chips [21] [22]. The component technology is the SmartPower (0.35 μm) from Motorola. Several blocks are specifically addressing the problematic of parasitic emission. One of the elementary structures has been designed to add a delay between the input and the output signals, and therefore to desynchronize digital block commutations. The time delay is controlled using 2 external DC voltages. The main feature of REGINA test chip is the emissive structure that has been designed to represent a simplified behavior of a microcontroller logic core. Several versions of this structure have been implemented in the test chip to cover the design rules we want to address. An on-chip sensor has been added to monitor internal currents within the die.

4.1. The Delay Structure :

The delay structure is able to introduce and control a delay to a signal, postponing the moment it changes of logic state (only for a transition from high to low state). The mechanism of this structure is to add a serial PMOS transistor on the path of the useful signal. The PMOS channel is used as a resistor controlled by the external V_{analog} voltage, that brakes the propagation of the signal in accordance with the V_{analog} voltage imposed on the PMOS gate. An inverter is then added to reformat the signal.

The adjunction of a NMOS transistor in parallel is necessary to increase the delay range of the structure (Figure 9). The couple of values (V_{analog} , V_{plage}) allows to specify a delay from a few picoseconds up to 45ns.

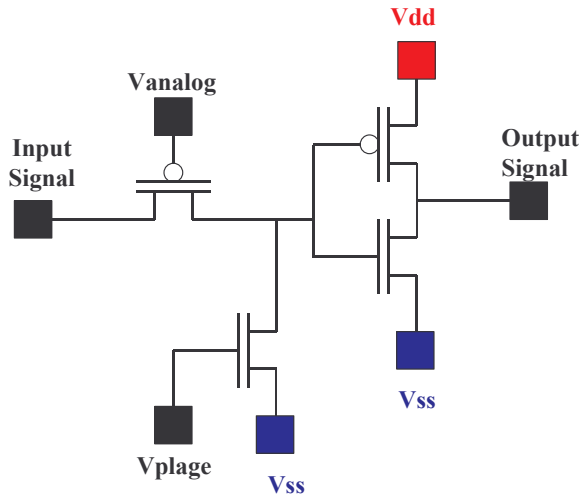


Figure 9 : Schematic of the delay structure

To calibrate this structure, we insert it in the dedicated oscillator circuit presented in Figure 10: the resulting frequency is externally measured (after a frequency divider allowing to output lower measurable frequencies). The delay introduced by the delay cell is then deduced from this output frequency. The curves (Figure 11) illustrate the functionality of this structure and its result voltages-delay conversion tables.

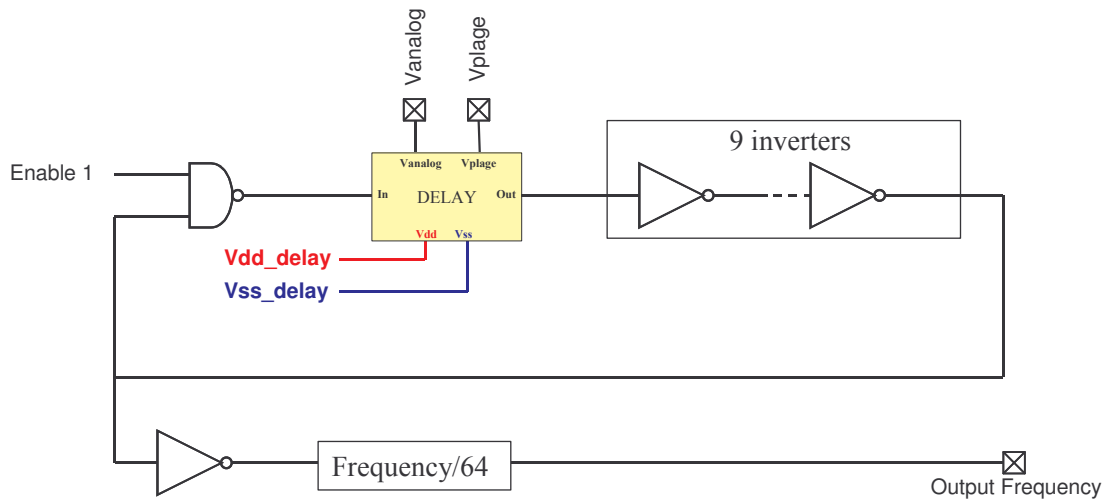
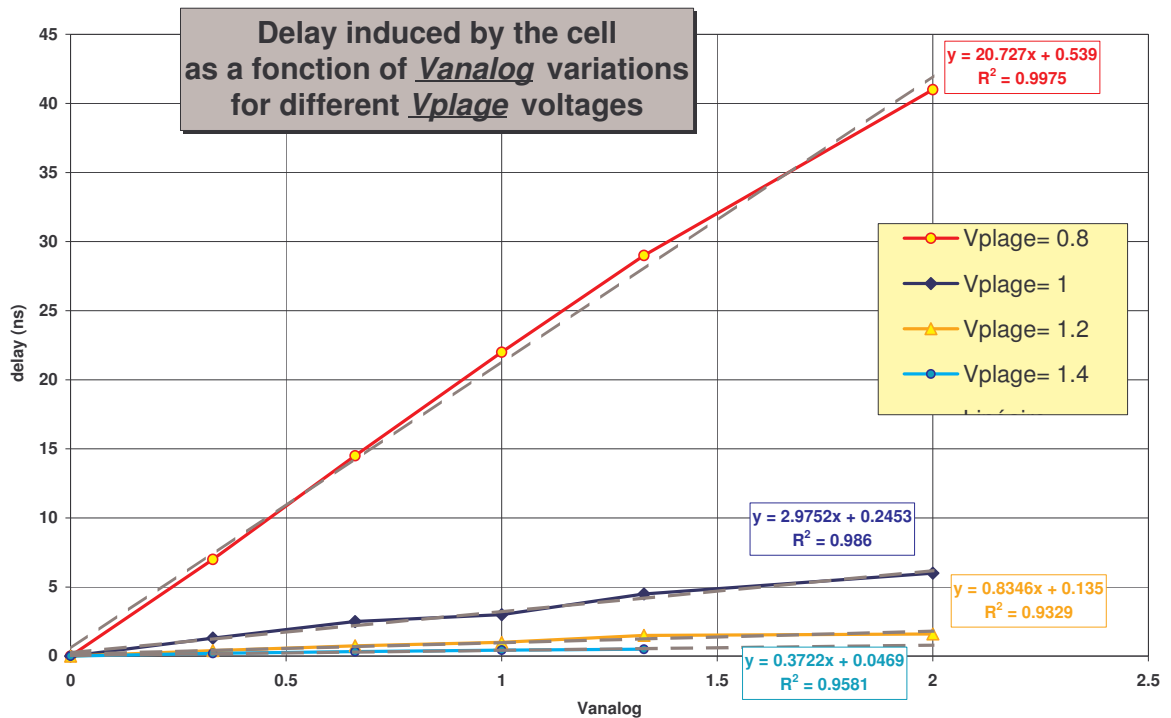


Figure 10 : Schematic for the calibration of the delay structure



| <i>Vanalog</i> (V) | <i>Vplage</i> (V) | Delais (ns) |
|--------------------|-------------------|-------------|
| -0,1 | 0,8 | 0,733611514 |
| -0,09 | 0,8 | 0,759182818 |
| -0,08 | 0,8 | 0,785645455 |
| -0,07 | 0,8 | 0,813030493 |
| -0,06 | 0,8 | 0,841370084 |
| -0,05 | 0,8 | 0,870697501 |
| -0,04 | 0,8 | 0,901047176 |

Look-up table between (*Vanalog*, *Vplage*) and real delay

Figure 11: Delay induced as a function of the 2 control voltages and associated look-up table.

4.2. The Emissive structure

The aim of the emissive structure is to reproduce the current consumption of a logic core on the power supply. The authors also chose to design a block which is easy to simulate. For that reason, the inverter has been chosen as the elementary device of the emissive structure. In order to have a realistic current consumption, the emissive structure had to be scalable: we implemented 3 chains of various number of inverters (4 inverters in the first chain, 16 in the second and 32 in the last). Each chain can be separately activated and a delay between them can be introduced by using the delay structure presented above. The Figure 12 is giving the electrical schematics of the structure. All outputs are observable externally on the printed circuit board and guaranty the functionality of the chip during the measurements.

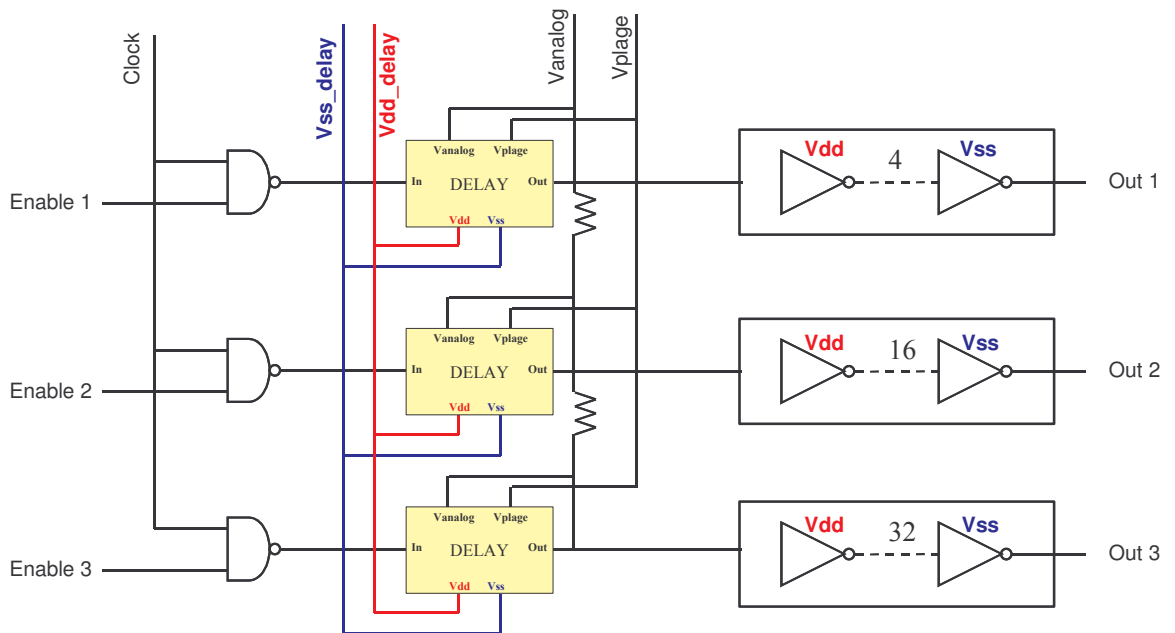


Figure 12 : Schematic of the emissive structure

4.3. The on-chip sensor

The on-chip sensor principle has been proposed for the first time in [23]. The sensor has here been redesigned in the Motorola 0.35 μ m SmartPower technology. Its principle uses the stroboscopic effect (Figure 13), thanks to the delay cell described in Section 4.1. The signal that has to be measured is a high frequency signal repeating itself at regular intervals. A sampling circuit (transmission gate and operational amplifier) captures this signal at the same repetition rate, but at each sampling a controlled delay is introduced on the sampling instant. Knowing this delay allows to reconstitute the high frequency signal. In our case, this signal is the noise observed on the on-chip power supplies; this noise is synchronized with the clock, occurring only at clock transition edges.

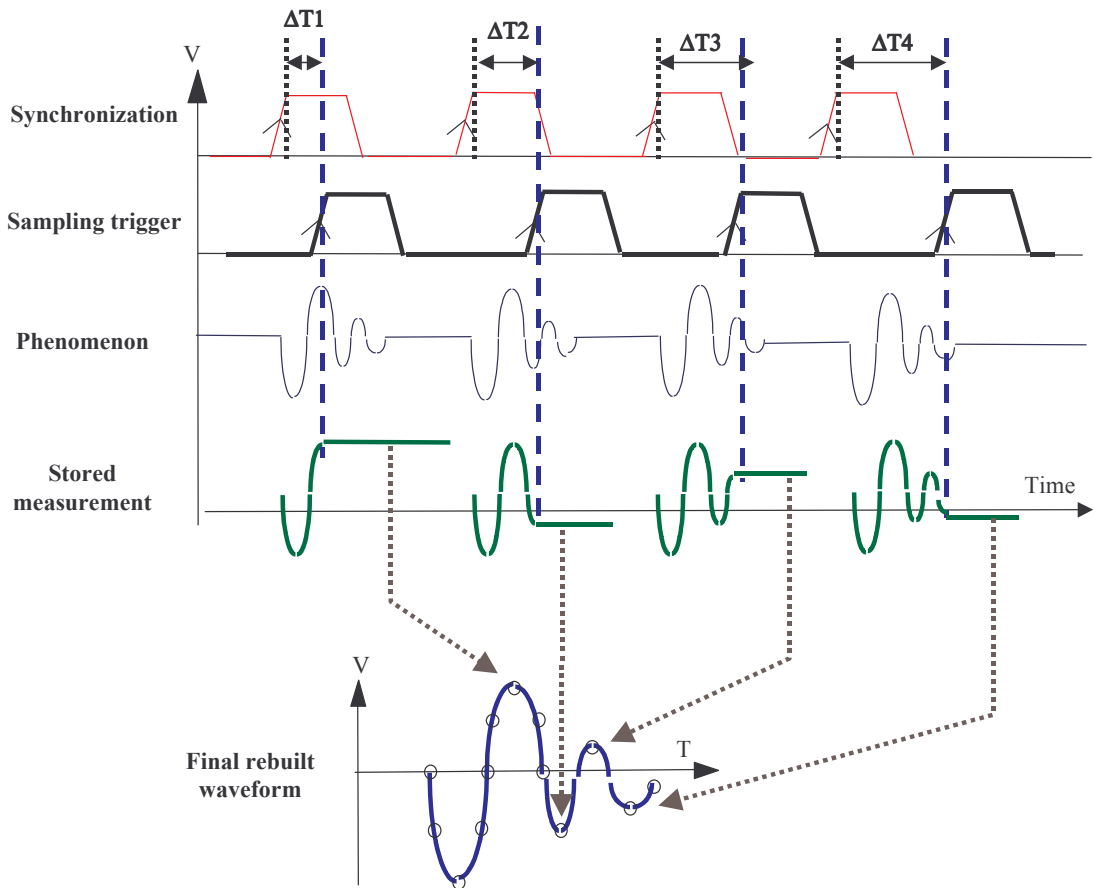


Figure 13: Measurement principle of the on-chip oscilloscope.

4.4. Layout of the test chip

The layout of the test mask is given on the Figure 14. Three emissive structures have been integrated. The first one is just a simple emissive structure. For the second one, we add scalable resistance on the power supply of the inverters and by using the on chip sensor, we are able to measure the internal current. For the third one, we add local decoupling capacitance on the power supplies of the inverters. This last structure is unfortunately not functional. Two calibration structures have also been added, one for the delay, the second one for the Operational Amplifier of the on-chip sensor.

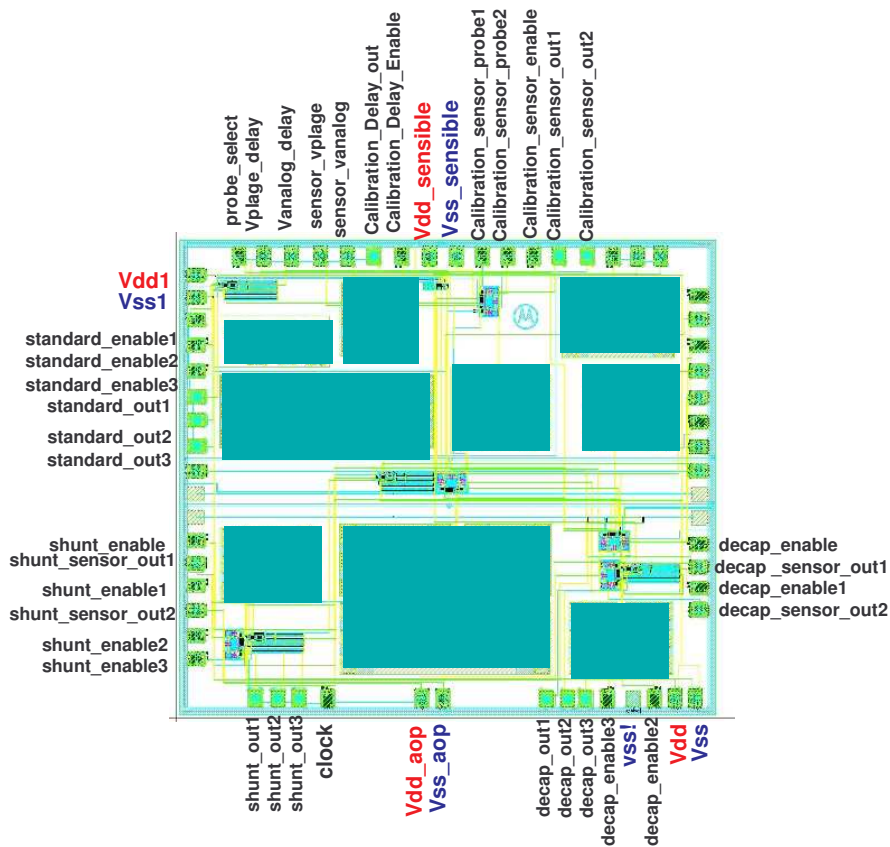


Figure 14 : Layout and Pin-Out of REGINA

In order to minimize the interference between the switching inverter noise, the control and measurement structures (delay cells, on-chip sampling), we separated the power supply in 3 isolated supply networks:

One supply for the emissive structures (VDD / VSS, VDD1 / VSS1) on which we can measure the internal current with the on-chip sensor.

One protected supply for feeding sensible structures such as delay structures and on-chip sensor

One specific supply for the Operational Amplifier in the on-chip sensor, which requires a higher voltage (4V) to get a measurement range from 0 to 3.3V.

Many pins are required to select the configuration of the test chip (enable, delay, ...) and most of these signals are monitored through a specific interface, as explained in the next sections. A particular pin is the clock one : in our test bench, the clock –i.e. the input of the emissive structure- is generated outside the device. Other pins are the outputs of the emissive structures and are used to verify the activation of the structures. The green boxes that can be seen on REGINA test mask layout (Figure 14) are not involved in the emission measurements and are Motorola Confidential Proprietary.

The package is a QLCC with 84 pins, which is more adapted to this test case than the TQFP one, that is of common use in automotive and wireless applications. Only 61 pins out of 84 are required for the parasitic emission measurement experiments.

5. Description of the PCB

We will here present the Printed Circuit Board that has been designed for the test mask. This PCB is used both for the conducted and radiated measurements described in the third section. The size of the PCB should therefore be 10x10 cm to be compatible with the TEM Cell requirements. The other constraints for the design of the PCB were to:

- allow separate activations of the emissive structures by switches
- allow connection or isolation of the different power supplies
- allow addition or removal of typical discrete loads
- allow monitoring of the on-chip sensor
- allow immunity measurements (which are not dealt with in this paper)

A picture of the PCB are given on the Figure 15. Because of the lack of space on the board, we chose to multiplex the observable signals in order to limit the number of connectors.

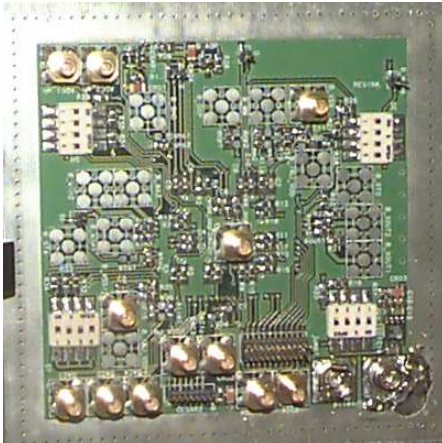


Figure 15 : Picture of both sides of the board

6. Test Bench Description

For emission measurements, many signals have to be monitored, such as activation of the emissive structures, time delay between the inverter chains, signals useful for the sensor on chip etc. All these constraints have lead us to develop a software to monitor the test chip by using available interface board named CESAR at the laboratory. This board has both the ADC and DAC capabilities. The Figure 16 illustrates the whole test bench.

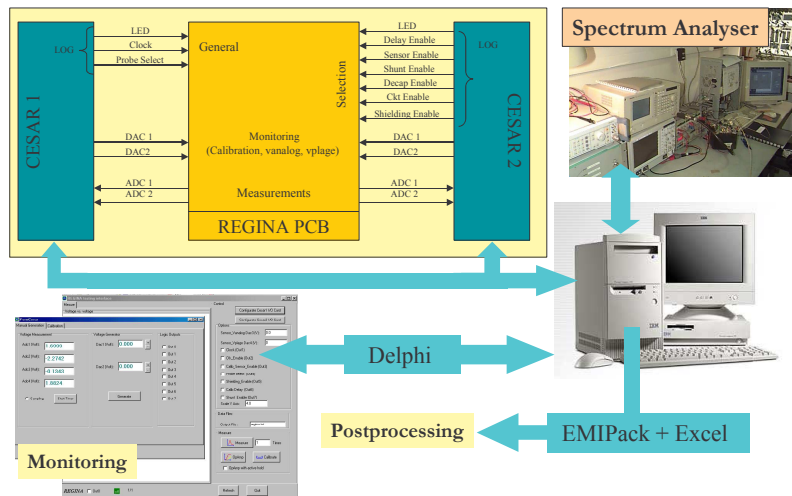


Figure 16 : REGINA test bench

The monitoring software has 3 main functions:

- it allows the various calibrations required, like delay cell or operational amplifier calibration
- when performing emission measurements with the spectrum analyzer, the software allows modifying the analog voltages (Vanalog & Vplage) that control the delay cell.
- for on-chip measurements using the current sensor, the software controls the sampling trigger by increasing the delay.

For each type of measurement, the software activates the appropriate REGINA structures through digital configuration signals.

7. Measurement Results

Main experiment results on parasitic emission using REGINA test chip are presented in this section, especially looking at clock frequency, delays and resistance parameters.

7.1. Variation of parasitic emission with the clock frequency

As the clock is externally provided to REGINA test chip, it is possible to vary the clock frequency using a frequency generator. The measured conducted emissions are given in Figure 17 for 2MHz, 8MHz and 26MHz clock frequencies: the whole emission spectrum level significantly raises (10dB μ V between 2 and 8MHz) with these clock frequency increases.

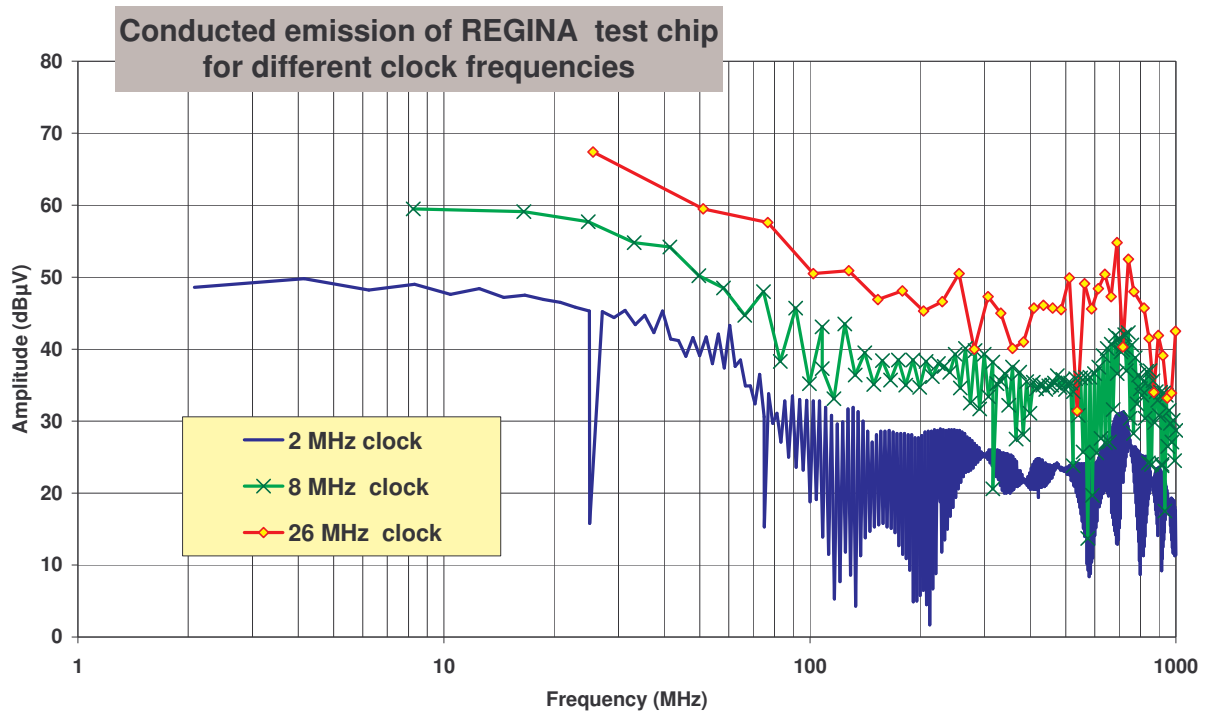


Figure 17: Measurement of the conducted emissions when varying the clock frequency

If we consider the amplitude of the clock first harmonic in the emission spectrum and plot it against the clock frequency, we observe (Figure 18-a) a logarithmic increase of this amplitude (in dBµV), which is in agreement with the results given by simple ICEM [24: Integrated Circuit Emission Model] model simulations (Figure 18-b). The straightforward design rule to minimize parasitic emissions is then to choose the lowest clock frequency that is required for the final application –which is often not the highest available frequency.

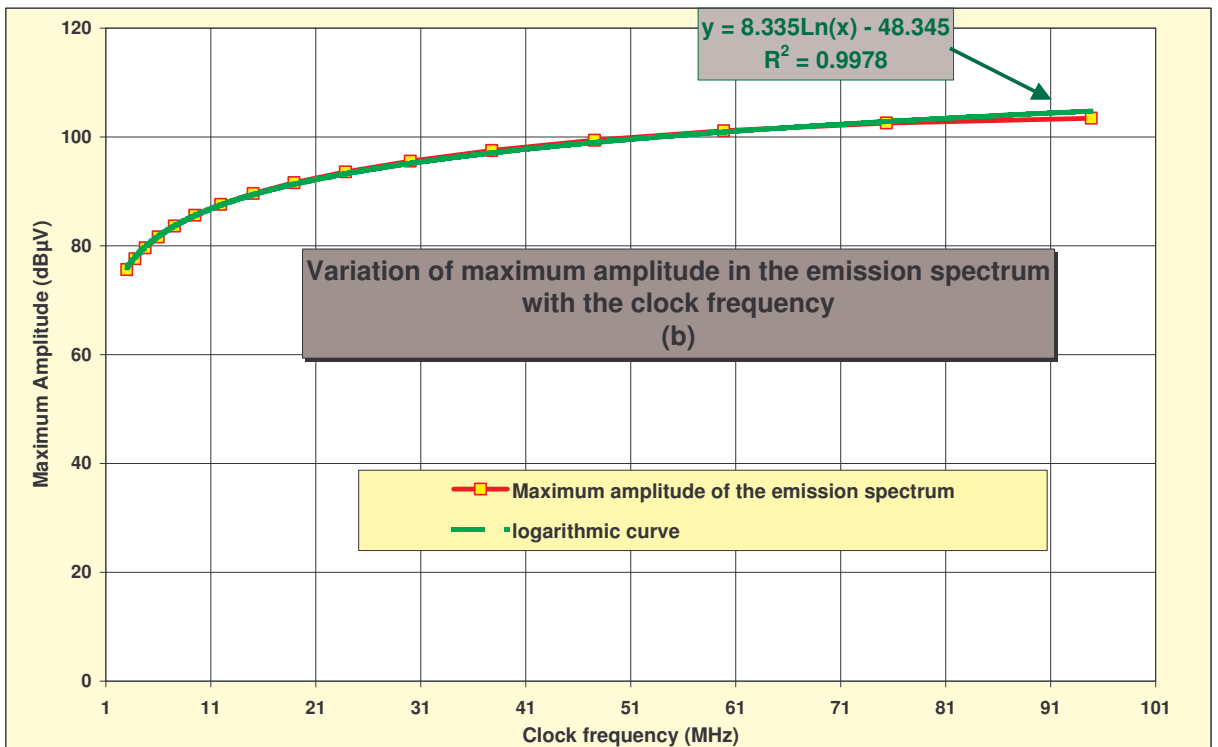
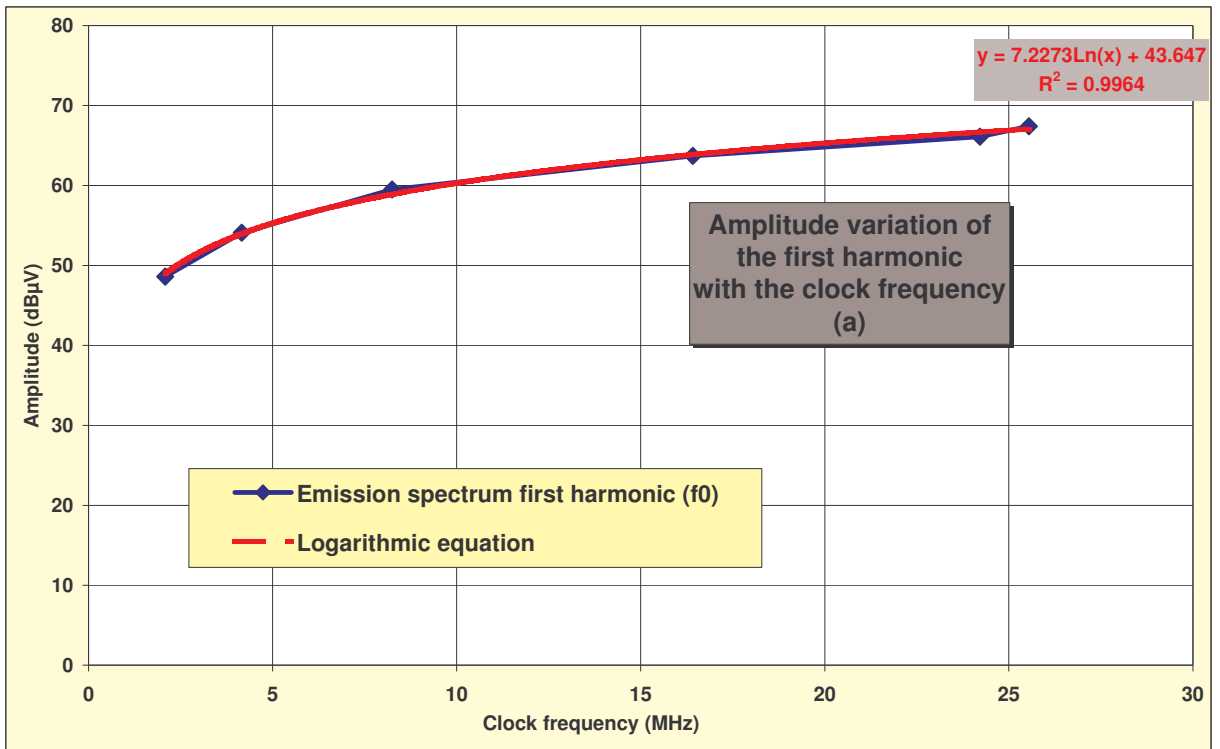
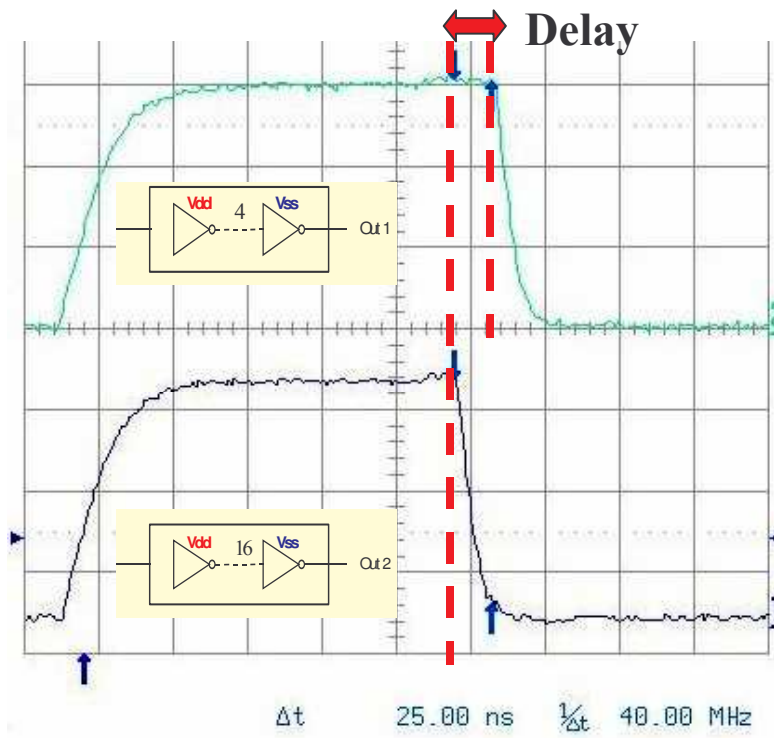


Figure 18: Amplitude variation of the emission spectrum first harmonic, in measurements (a) and in simulations (b)

7.2. Variation of parasitic emission with delay introduction

One of the exploitation of this test chip is to verify the influence of the digital signal synchronization on the power consumption. The experiment consists in adding a delay between signals of the three inverter blocks in the standard emissive structure. The output time curves of two blocks with delay are given on Figure 19. The delay between the two output signals occurs only on the signal falling edge, while the rising edges are kept synchronous: this results in modifying the duty cycle of the delayed signal.



Output voltages

Figure 19 : Two Delayed Outputs

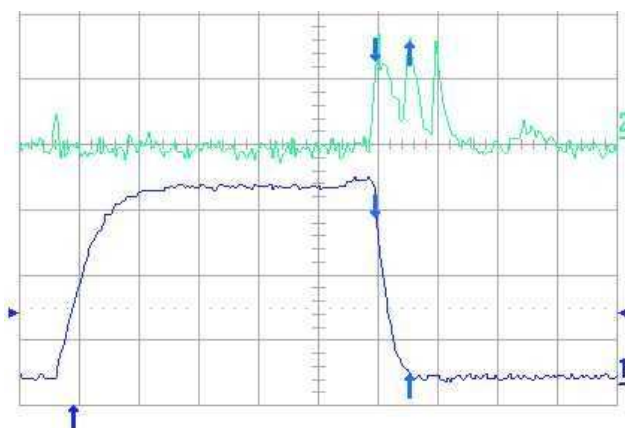


Figure 20 : Current measured on the 1 Ohm resistance

The current measured on the 1 Ohm resistance that is set on the external Vss supply track is shown on Figure 20: three distinct current peaks can be observed, each one corresponding to a signal transition (and therefore to inverter's switching) in one of the three inverter blocks.

If we compare the cases without and with introduction of a delay between 2 inverter blocks (see Figure 21), we observe that the spectrum measured with a delay (dotted curve) presents clear lower emission levels at some particular frequencies or frequency bands.

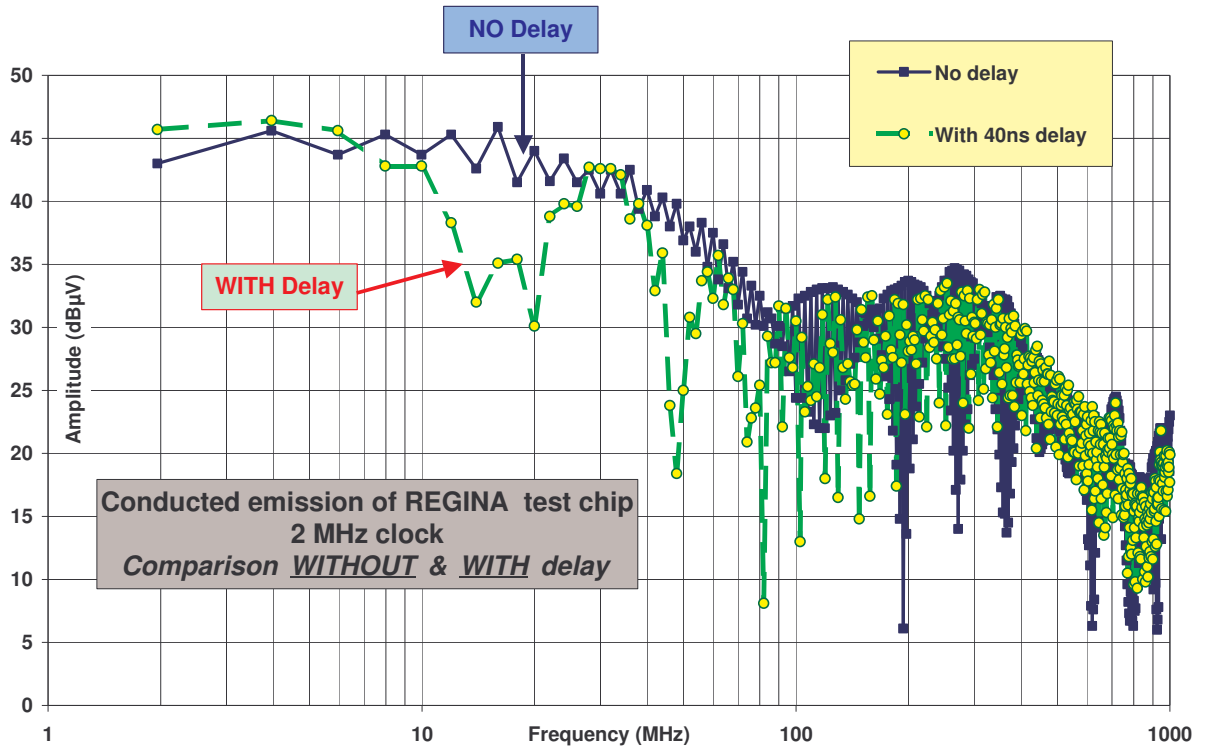


Figure 21 : Conducted measurement (IEC61967-4): with and without a delay

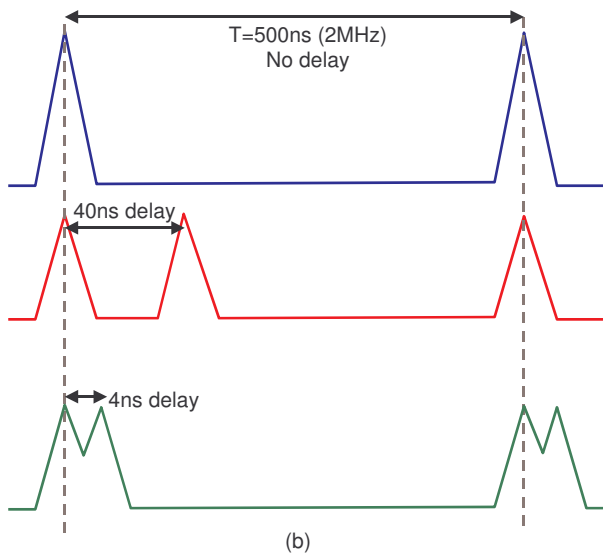
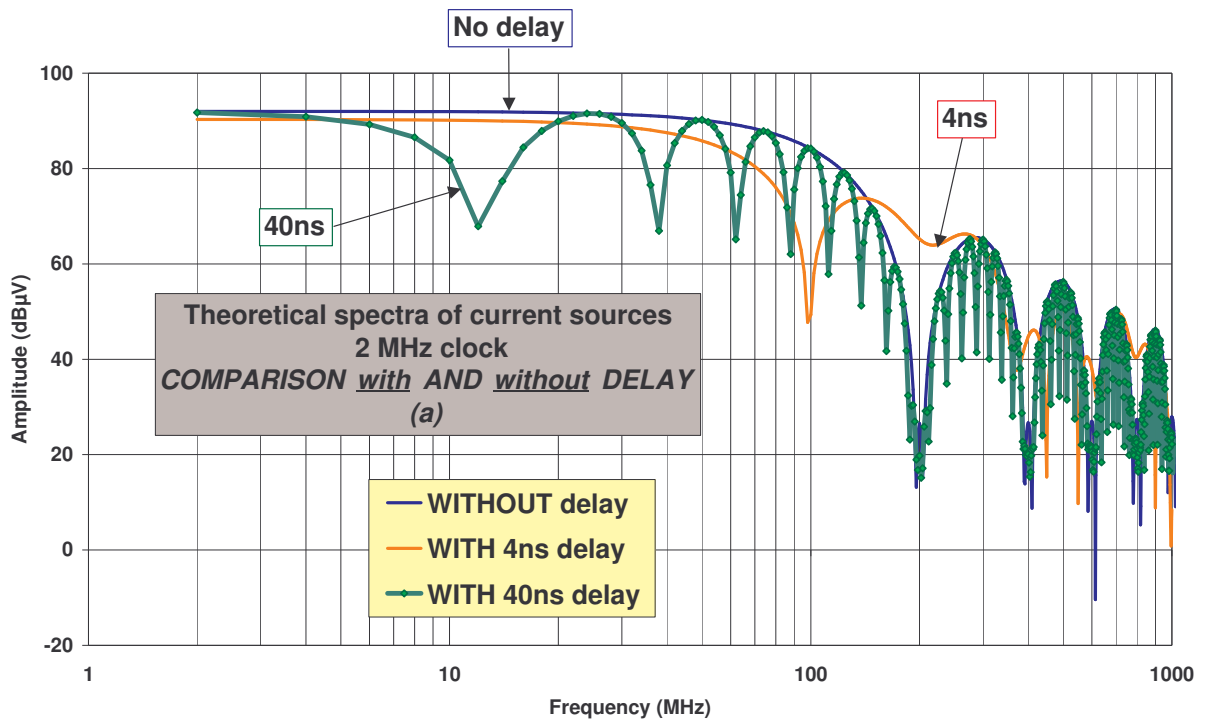


Figure 22: Theoretical emission spectra (a) of different current peak shapes (b)

Such emission spectra can be reproduced in simulation (Figure 22-left) with the appropriate current peak shapes (Figure 22-right).

Looking at the amplitude of the 3 first harmonics of the measured emission spectra as functions of the induced delays, we obtain the plot in Figure 23. By comparing to the amplitudes measured when no delay is introduced, we can determine that a reduction of emission of a few dBµV occurs for small delays (smaller than $1/20^{\text{th}}$ of the clock period), and that no such reduction is obvious for longer delays.

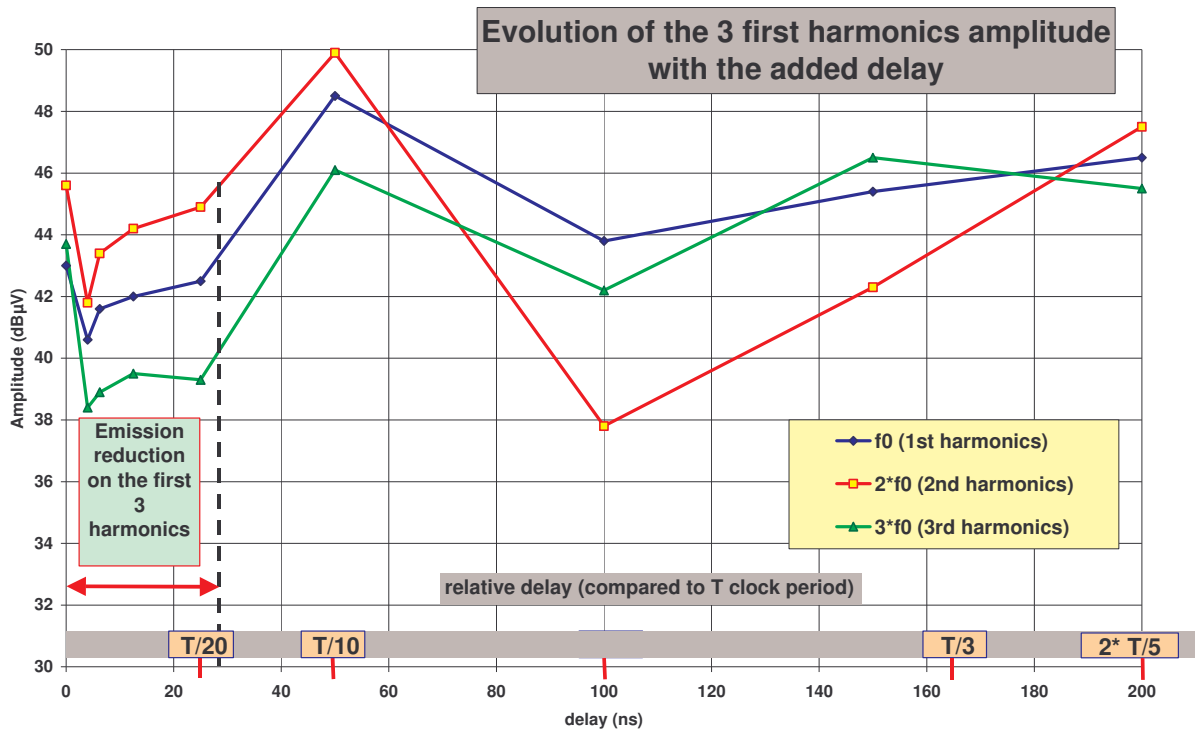


Figure 23: First harmonic amplitude variation with the induced delay

The gain observed in the reduction of emission by addition of delays between signals is then limited to narrow frequency bands, making the trade-off between emission reduction and cost of development/use of the delay cell worth only for a few applications (power devices...) that need improvements at very specific frequencies. Moreover, only small delays (compared to the clock period) will offer some gain for the first harmonics of the spectrum.

7.3. Variation of parasitic emission with power supply resistance

In this paragraph, we will compare the emission of the shunt emissive structure (dotted curve in Figure 22) and standard emissive structure (solid curve in Figure 22). The difference between the two structures is the insertion of a 4.3 Ohm resistance on the Vdd and Vss power supply tracks in the case of the shunt structure. The clock frequency is fixed at 2 MHz, all the outputs of the emissive structures are connected to an external 10pF capacitance. No delay has been introduced for these measurements.

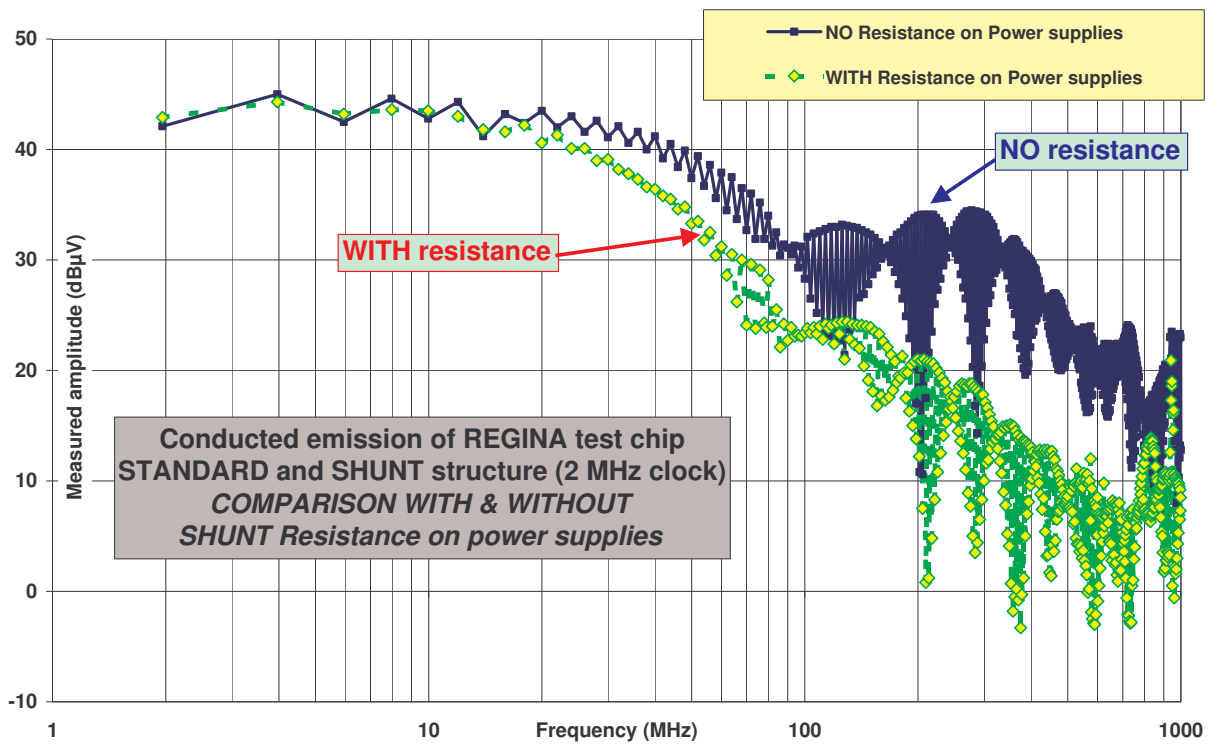


Figure 24 : Conducted measurement (IEC61967-4): with and without a resistance on the power supply

For the conducted measurement (see Figure 24), the influence of the serial resistance is rather positive on the emissive spectrum: the reduction of the amplitude level is about $10\text{dB}\mu\text{V}$ in average over a wide frequency range, starting from 20MHz up to 1GHz.

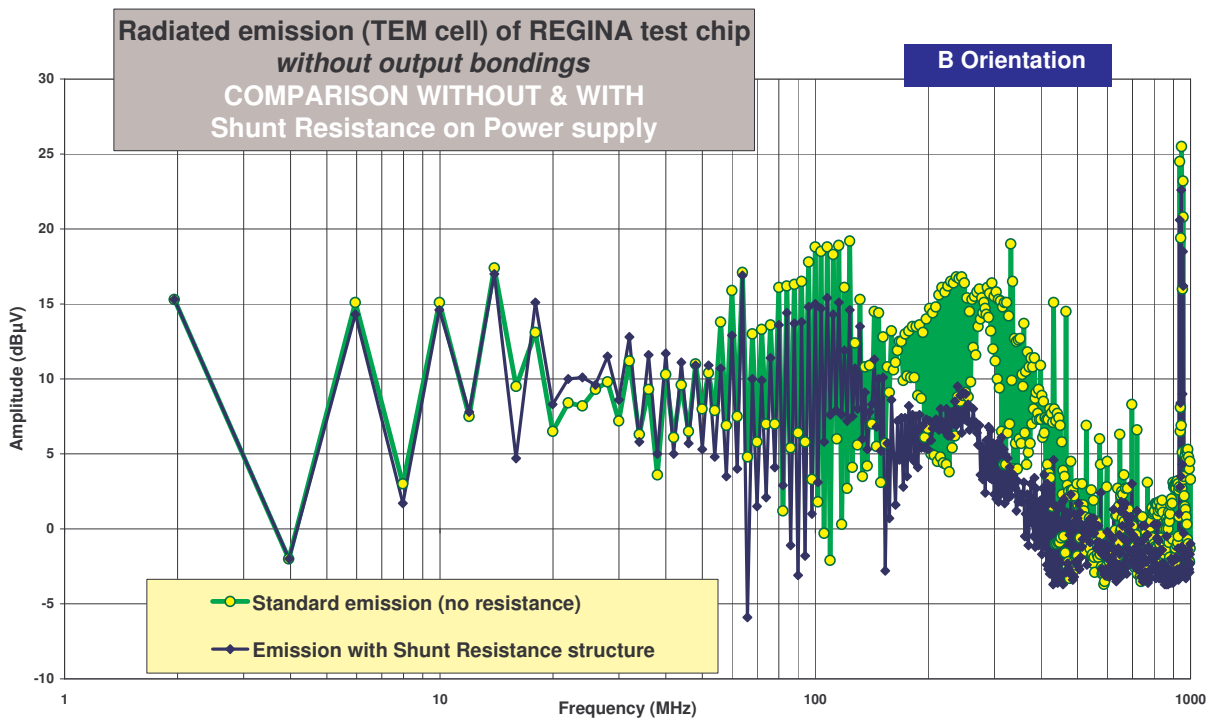
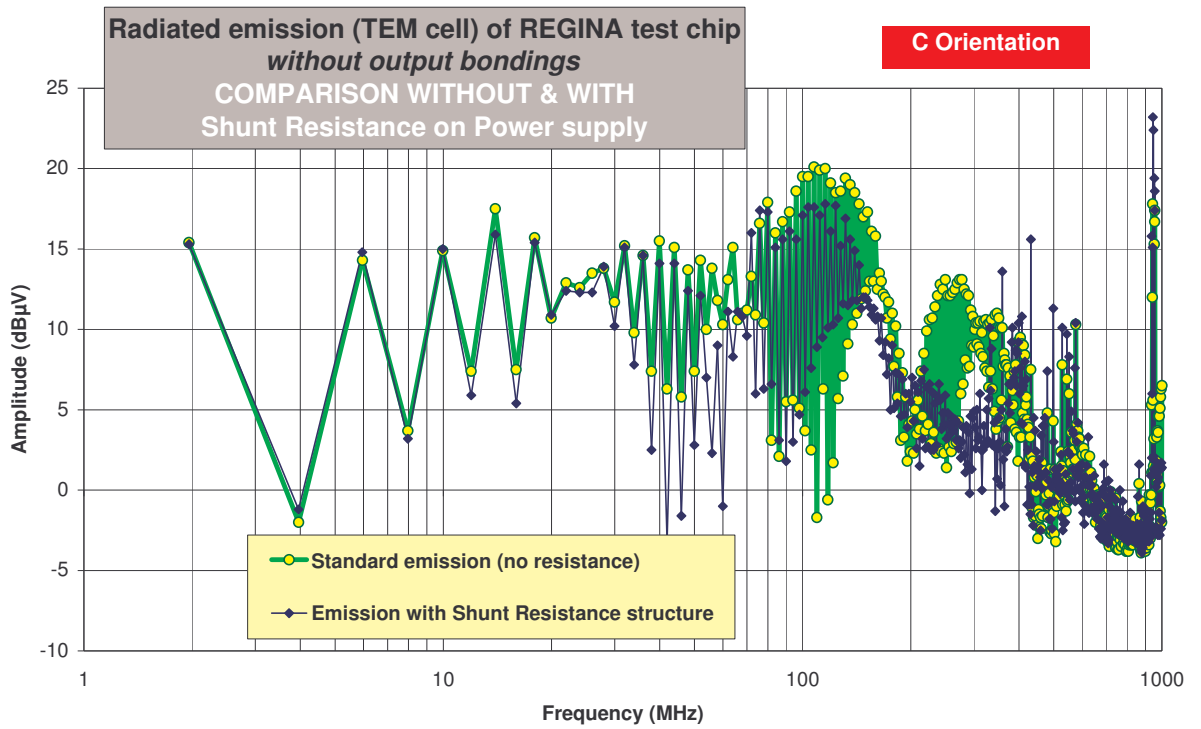


Figure 25 : Radiated Measurement (IEC61967-2) (in 2 orientations of the board): with and without a resistance

Impact of the resistance on radiated measurement is not as obvious. Output signals of the emissive structures towards the PCB and external loads had to be removed in order not to hide the power supply noise. The measured spectra for two board

orientations are presented in Figure 25, once this modification done. An improvement is observed in higher frequencies (around 100MHz and 400MHz) but is of smaller magnitude than in conducted emissions.

7.4. On-chip sensor measurements

Measurements of the internal noise propagated on the power supply rails have been realized using the on-chip sensor. Results are presented in Figure 26: the red curve is the measurement with the on-chip sensor of the internal current peak on the power supply rail, and the green curve is the same current measured with the oscilloscope on the 1 Ohm probe on the board. A good correlation of shape (length, rising and falling times) are found between the two measurements, but the current maximum amplitude measured inside the chip is about 3 times higher than the one measured outside of the chip: internal currents are attenuated by elements on their propagation path, like on-chip intrinsic capacitance, or external decoupling capacitances.

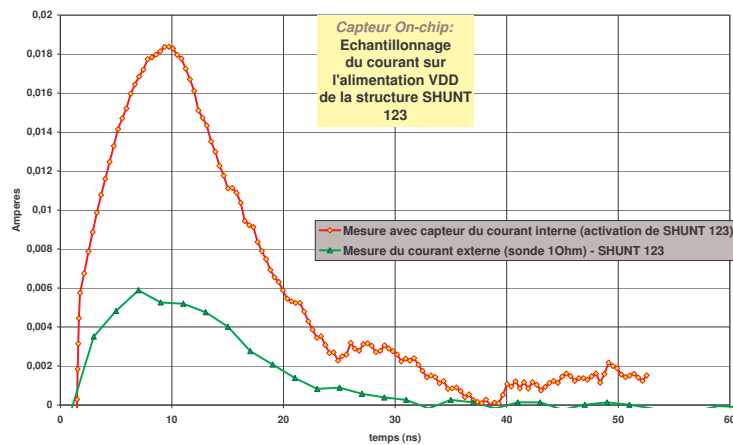


Figure 26: On-chip measurement of parasitic emissions, compared to external measurements.

Such a measurement is a promising result for parasitic emission modeling and may be used for the new ICEM standard emission model [24] [25] to implement parameters like the noise current source. Using the on-chip sensor may also allow characterizations of dynamic current consumption and validations of large chips in an industrial design flow, especially when EMC requirements are strong like in the transportation industry.

8. Conclusion

This article has presented the measurement results obtained by a test chip named REGINA. The objective of such component, fabricated in Motorola SmartPower 0.35 μ m technology, was the validation of guidelines allowing to improve the EMC behavior of integrated circuits used for automotive applications. Origins and main measurements methods of the IC parasitic emissions have been presented. REGINA specifications and main features, like delay cell, emissive structure and on-chip sensor, have been described. The specific board and measurement bench developed for the component testing have been detailed. The main measurements results achieved with this chip advocate for the choice of the lowest required clock frequency to lower parasitic

emissions and for the use of a serial resistance on power supplies, but show no clear improvement when adding delays between structures. Measurements realized with the on-chip current sensor will help in modeling internal parasitic currents as per IEC standard.

Acknowledgements :

We want to give special thanks to the designers of the Motorola automotive group in Toulouse, who have supported us for the design of this test mask.

Many thanks as well to Stephane Baffreau at INSA-LESIA, for his help and support on the measurements.

Appendices:

The measured spectra presented in this paper have actually been processed for an easier presentation: the raw measured spectra display many frequency points that are of no direct interest, since the whole emitted spectrum of a synchronous component is made of harmonics (and sub-harmonics) of the clock frequency. By keeping only these harmonics (4MHz in the case of Figure 27), we obtain the envelope of the emission spectrum. Such a post-processing makes the understanding of measurements results and comparison easier and does save data memory space.

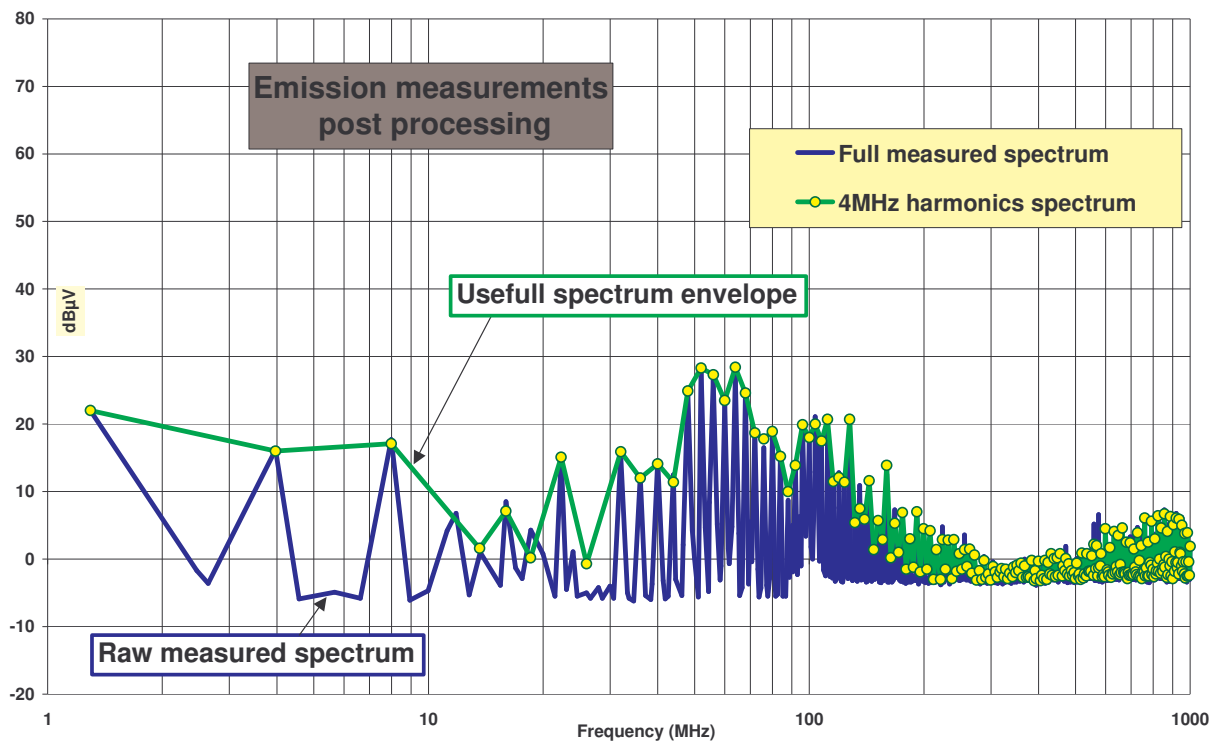


Figure 27: Post-processing of the measured spectra allows to retain only the envelope of emission spectra.

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